Fig.1

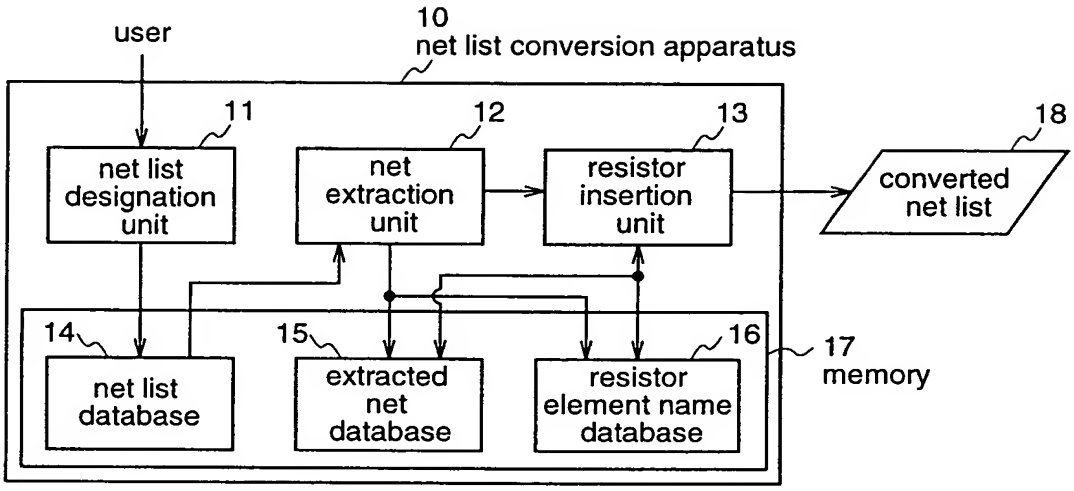
user
10
net list conversion apparatus
11
12
13
18
net list designation unit
net extraction unit
resistor insertion unit
converted net list
14
15
16
17
memory
net list database
extracted net database
resistor element name database

Fig.2

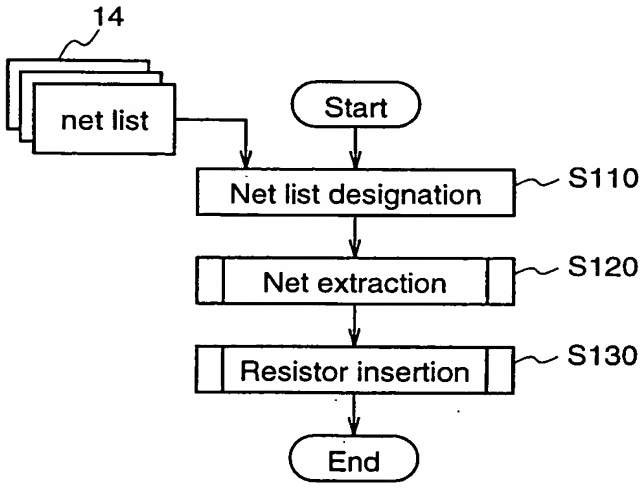
14
net list
Start
Net list designation
S110
Net extraction
S120
Resistor insertion
S130
End

Fig.3

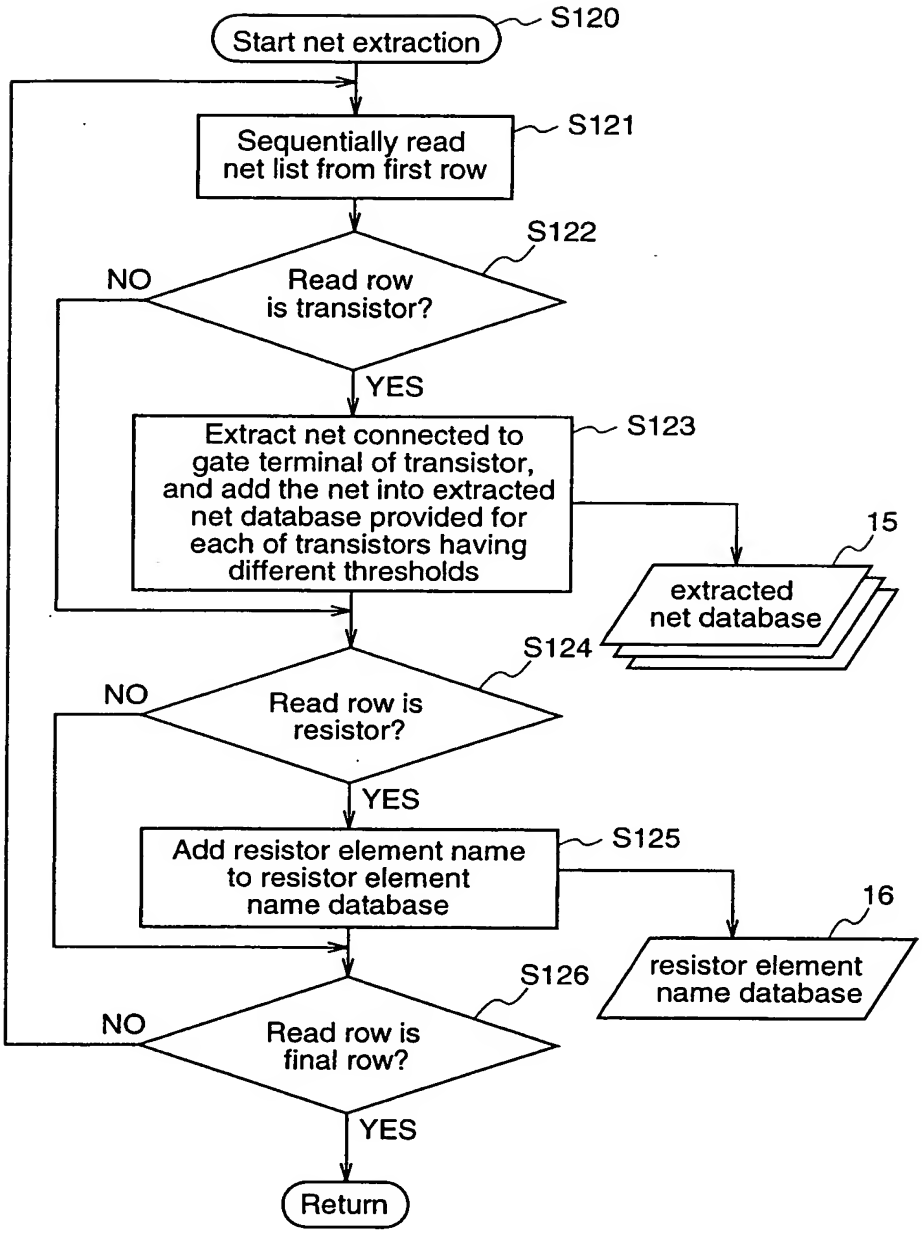
Start net extraction
S120
Sequentially read net list from first row
S121
Read row is transistor?
S122
NO
YES
Extract net connected to gate terminal of transistor, and add the net into extracted net database provided for each of transistors having different thresholds
S123
15
extracted net database
Read row is resistor?
S124
NO
YES
Add resistor element name to resistor element name database
S125
16
resistor element name database
Read row is final row?
S126
NO
YES
Return

Fig.4

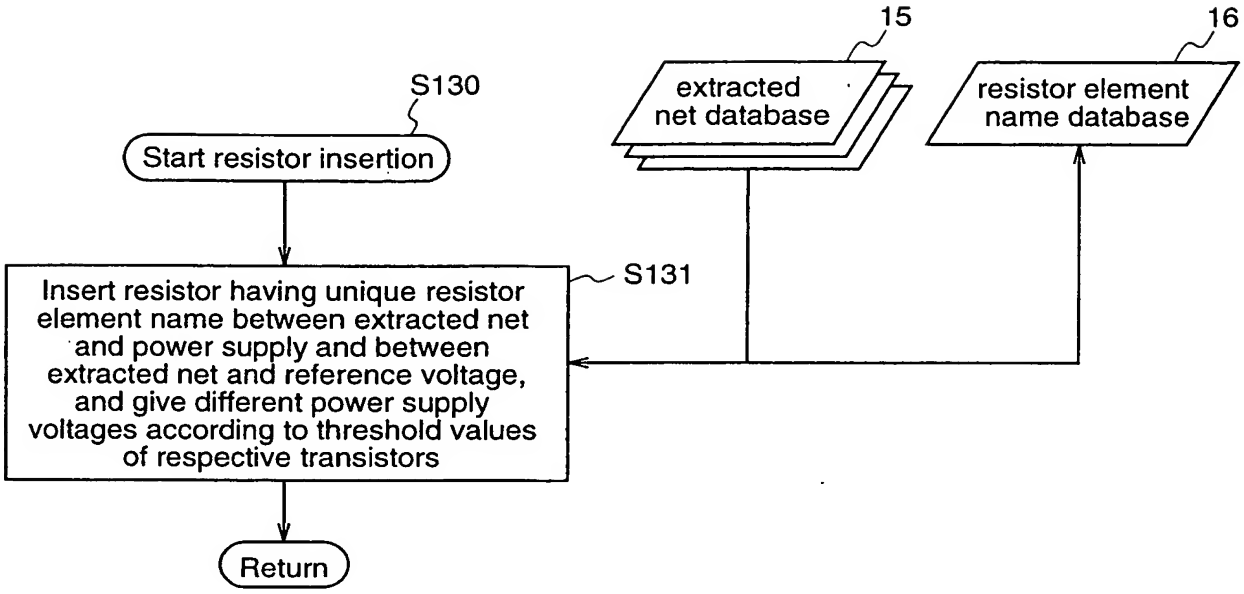

Fig.5(a)

target net list 14

```
1.    MP1 c c AVDD AVDD pchhvt l=1u w=5u
2.    MN1 c a b      0     nchhvt l=1u w=5u
3.    R1   b 0 10k
4.    XOP1 VREF b a ENABLE1 OP
5.
6.    MP2 DOUT d VDD VDD pchlvt l=1u w=2u
7.    MN2 DOUT d 0    0     nchlvt l=1u w=1u
8.    XTBUF1 DIN d ENABLE2 TBUF
9.
10.   .SUBCKT OP P N A E
11.   MP01 1 2 3 4 pchhvt l=1u w=5u
12.   MN01 5 6 7 8 nchhvt l=1u w=5u
13.      :
14.   .END OP
15.
16.   .SUBCKT TBUF IN OUT E
17.   MP01 1 2 3 4 pchlvt l=1u w=2u
18.   MN01 5 6 7 8 nchlvt l=1u w=1u
19.      :
20.   .END TBUF
21.
22.   .end
```

Fig.5(b)

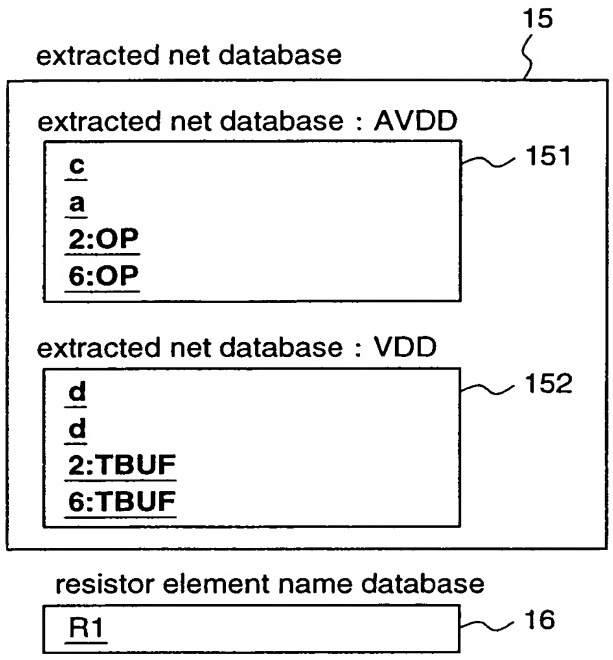
15
extracted net database
extracted net database : AVDD
c
a
2:OP
6:OP
151
extracted net database : VDD
d
d
2:TBUF
6:TBUF
152
resistor element name database
R1
16

Fig.5(c)

post-conversion net list

18

```
1.   MP1 c c AVDD AVDD pchhvt l=1u w=5u
2.   MN1 c a b      0      nchhvt l=1u w=5u
3.   R1   b 0 10k
4.   XOP1 VREF b a ENABLE1 OP
5.
6.   MP2 DOUT d VDD VDD pchlvt l=1u w=2u
7.   MN2 DOUT d 0    0     nchlvt l=1u w=1u
8.   XTBUF1 DIN d ENABLE2 TBUF
9.
10.  .SUBCKT OP P N A E
11.  MP01 1 2 3 4 pchhvt l=1u w=5u
12.  MN01 5 6 7 8 nchhvt l=1u w=5u
13.     :
14.  R0P000 2 AVDD 100T
15.  R0P001 2 0    100T
16.  R0P002 6 AVDD 100T
17.  R0P003 6 0    100T
18.  .END OP
19.
20.  .SUBCKT TBUF IN OUT E
21.  MP01 1 2 3 4 pchlvt l=1u w=2u
22.  MN01 5 6 7 8 nchlvt l=1u w=1u
23.     :
24.  RTBUF000 2 VDD 100T
25.  RTBUF001 2 0   100T
26.  RTBUF002 6 VDD 100T
27.  RTBUF003 6 0   100T
28.  .END TBUF
29.
30.  R1000 c AVDD 100T
31.  R1001 c 0    100T
32.  R1002 a AVDD 100T
33.  R1003 a 0    100T
34.  R1004 d VDD  100T
35.  R1005 d 0    100T
36.  R1006 d VDD  100T
37.  R1007 d 0    100T
38.
39.  .end
```

16'

resistor element name database

R1
R0P000:OP
R0P001:OP
R0P002:OP
R0P003:OP
RTBUF000:TBUF
RTBUF001:TBUF
RTBUF002:TBUF
RTBUF003:TBUF
R1000
R1001
R1002
R1003
R1004
R1005
R1006
R1007

Fig.6

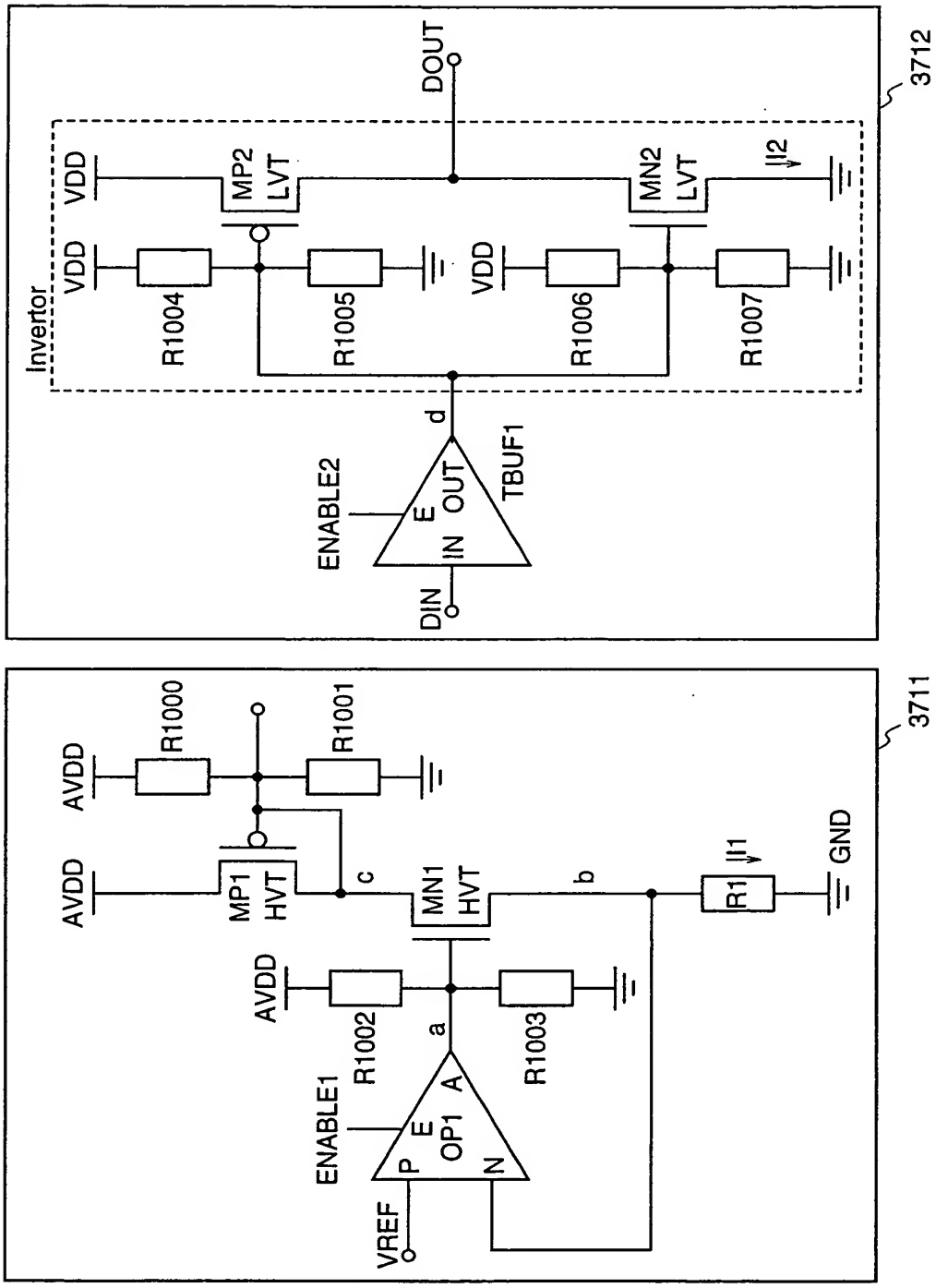
3712
DOUT
VDD
MP2
LVT
MN2
LVT
I2
Invertor
VDD
R1004
R1005
VDD
R1006
R1007
d
ENABLE2
E
OUT
TBUF1
IN
DIN
3711
R1000
R1001
AVDD
AVDD
MP1
HVT
c
MN1
HVT
b
R1
I1
GND
AVDD
R1002
a
R1003
ENABLE1
P
E
OP1
A
N
VREF

Fig.7

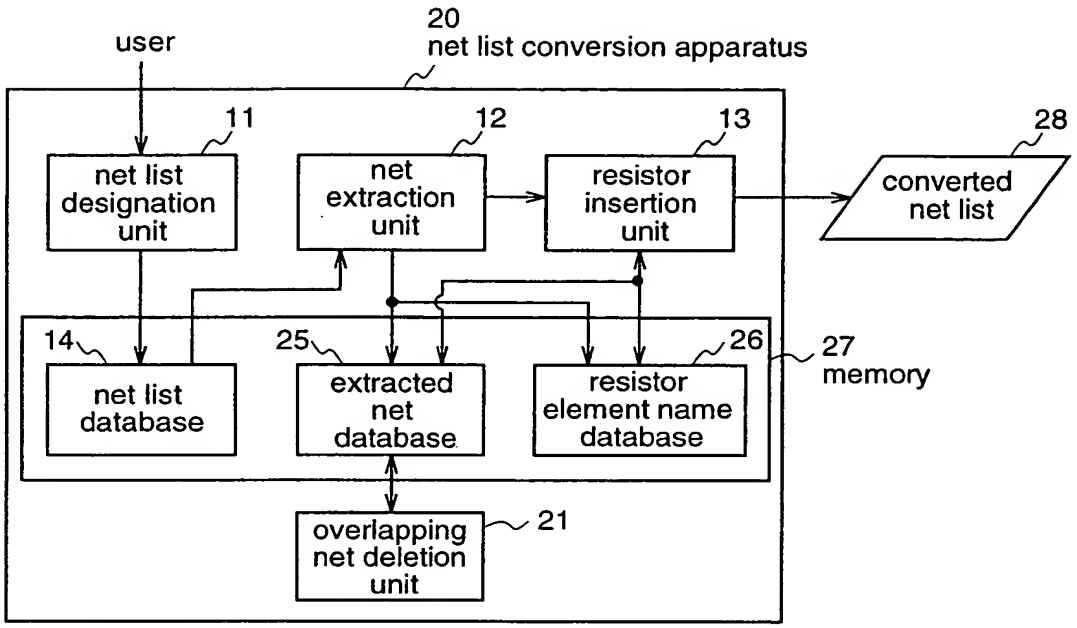
user
20
net list conversion apparatus
11
12
13
28
net list designation unit
net extraction unit
resistor insertion unit
converted net list
14
25
26
27
memory
net list database
extracted net database
resistor element name database
overlapping net deletion unit
21

Fig.8

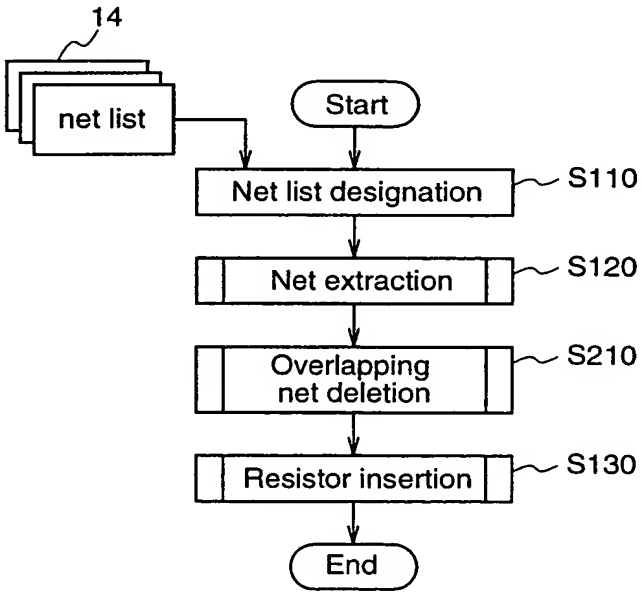
14
net list
Start
Net list designation
S110
Net extraction
S120
Overlapping net deletion
S210
Resistor insertion
S130
End

Fig.9

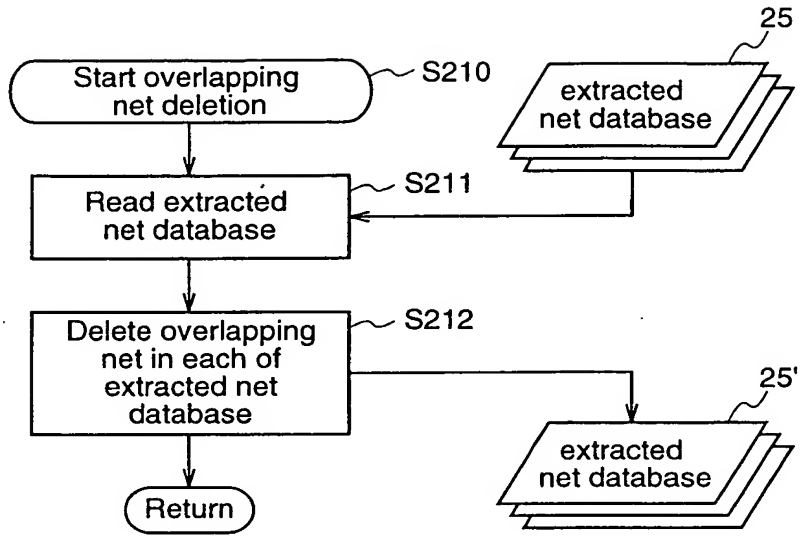
Start overlapping net deletion
S210
Read extracted net database
S211
Delete overlapping net in each of extracted net database
S212
Return
25
extracted net database
25'
extracted net database

Fig.10(a)

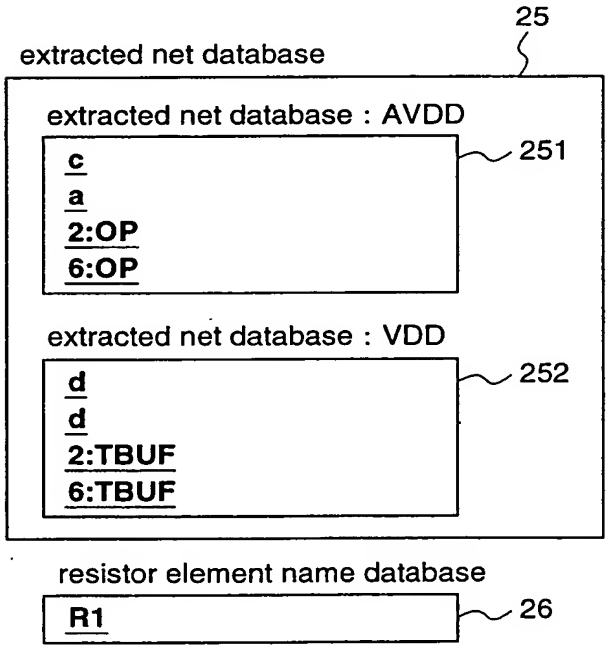
25
extracted net database
extracted net database : AVDD
c
a
2:OP
6:OP
251
extracted net database : VDD
d
d
2:TBUF
6:TBUF
252
resistor element name database
R1
26

Fig.10(b)

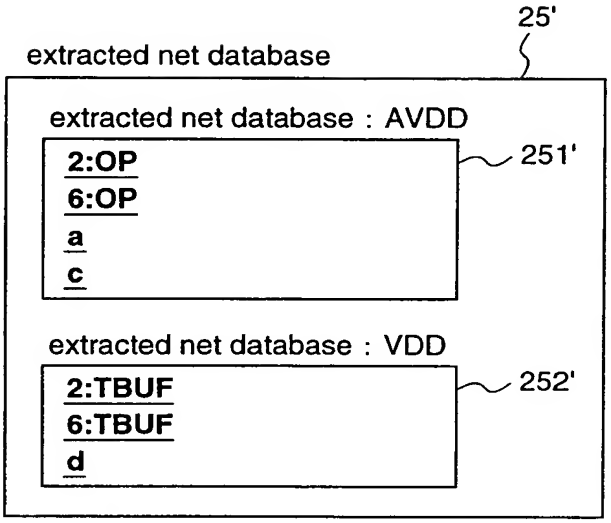
25'
extracted net database
extracted net database : AVDD
2:OP
6:OP
a
c
251'
extracted net database : VDD
2:TBUF
6:TBUF
d
252'

Fig.10(c)

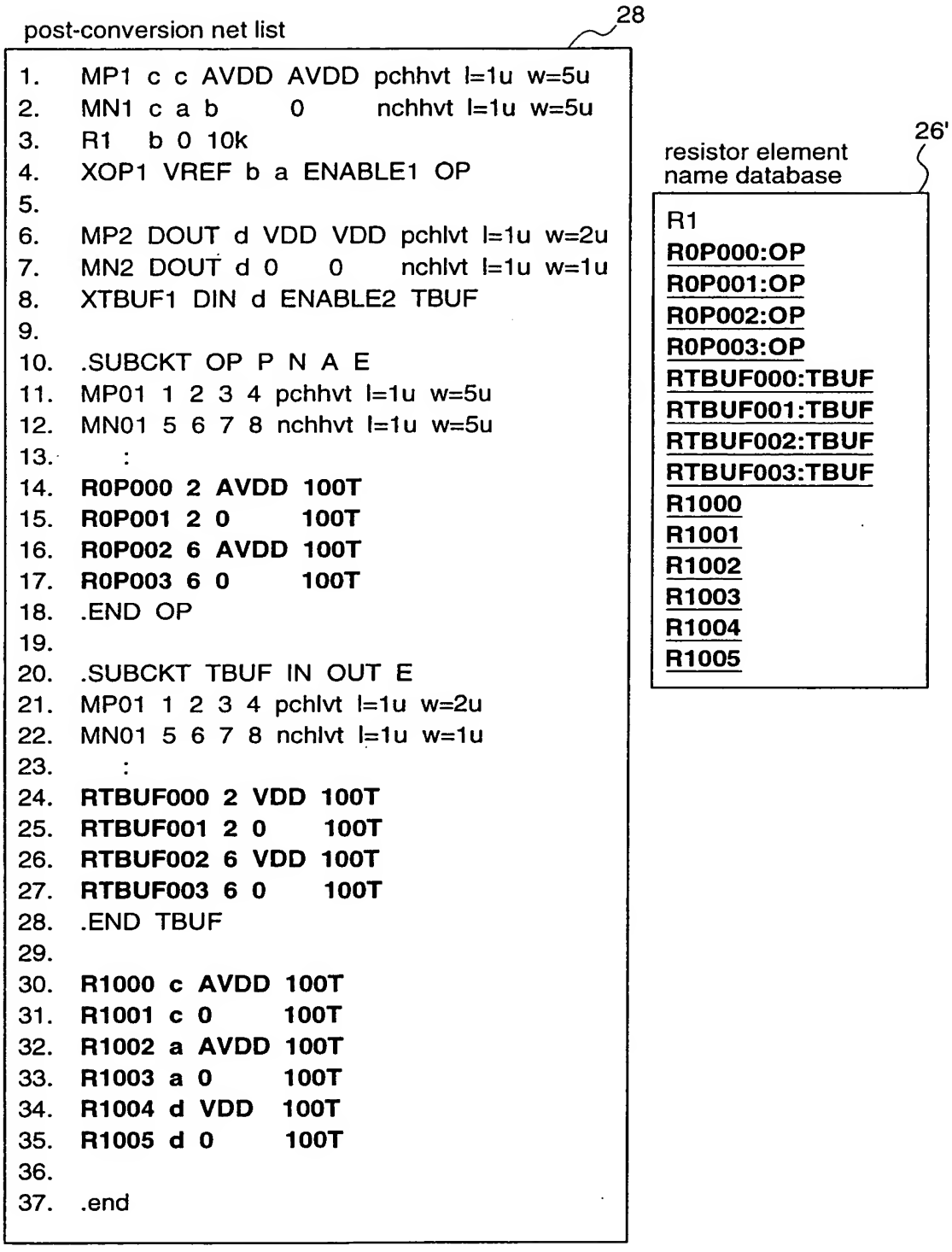
post-conversion net list
28
1. MP1 c c AVDD AVDD pchhvt l=1u w=5u
2. MN1 c a b 0 nchhvt l=1u w=5u
3. R1 b 0 10k
4. XOP1 VREF b a ENABLE1 OP
5.
6. MP2 DOUT d VDD VDD pchlvt l=1u w=2u
7. MN2 DOUT d 0 0 nchlvt l=1u w=1u
8. XTBUF1 DIN d ENABLE2 TBUF
9.
10. .SUBCKT OP P N A E
11. MP01 1 2 3 4 pchhvt l=1u w=5u
12. MN01 5 6 7 8 nchhvt l=1u w=5u
13. :
14. R0P000 2 AVDD 100T
15. R0P001 2 0 100T
16. R0P002 6 AVDD 100T
17. R0P003 6 0 100T
18. .END OP
19.
20. .SUBCKT TBUF IN OUT E
21. MP01 1 2 3 4 pchlvt l=1u w=2u
22. MN01 5 6 7 8 nchlvt l=1u w=1u
23. :
24. RTBUF000 2 VDD 100T
25. RTBUF001 2 0 100T
26. RTBUF002 6 VDD 100T
27. RTBUF003 6 0 100T
28. .END TBUF
29.
30. R1000 c AVDD 100T
31. R1001 c 0 100T
32. R1002 a AVDD 100T
33. R1003 a 0 100T
34. R1004 d VDD 100T
35. R1005 d 0 100T
36.
37. .end
resistor element name database
26'
R1
R0P000:OP
R0P001:OP
R0P002:OP
R0P003:OP
RTBUF000:TBUF
RTBUF001:TBUF
RTBUF002:TBUF
RTBUF003:TBUF
R1000
R1001
R1002
R1003
R1004
R1005

Fig.11

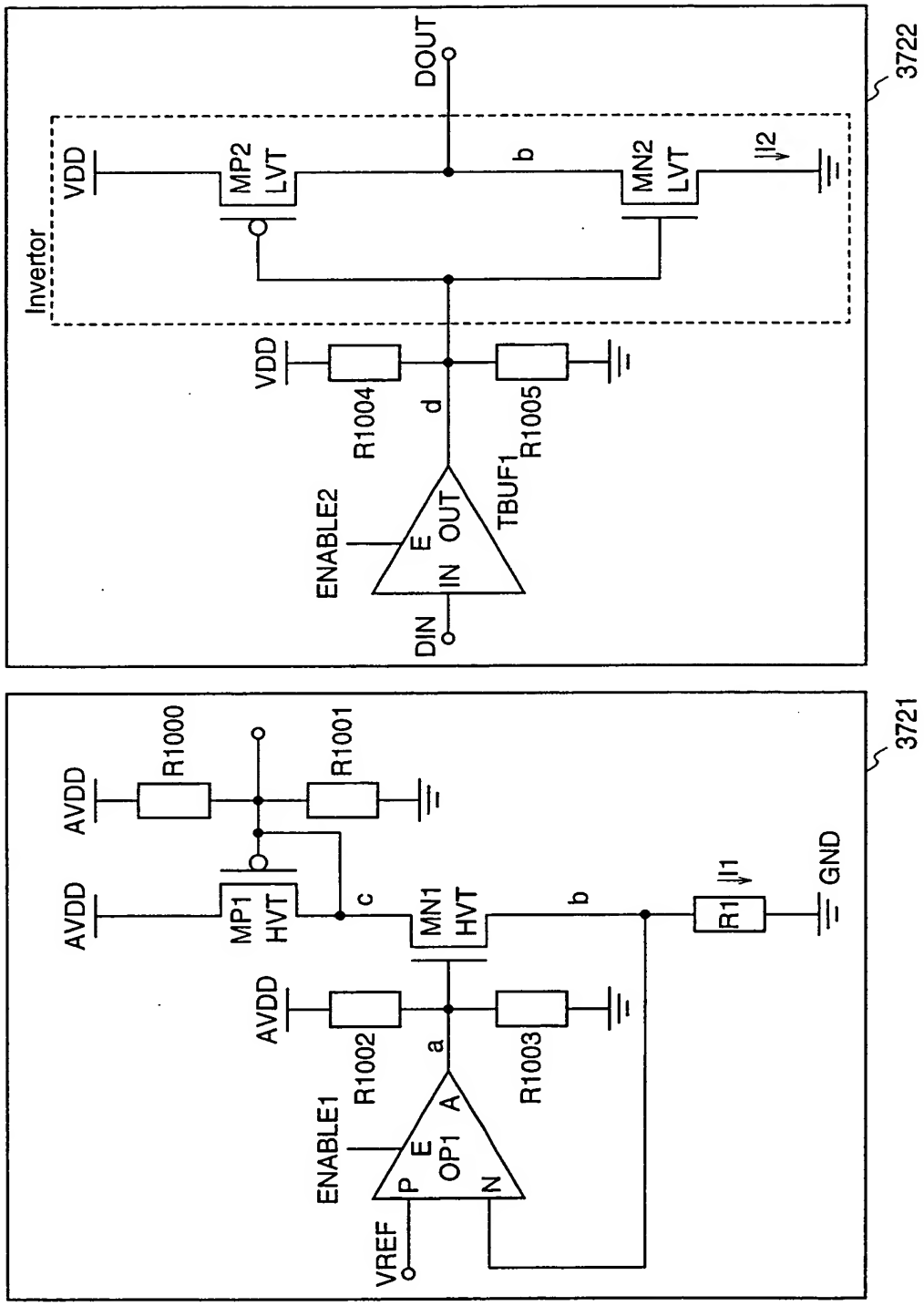
3722
DOUT
VDD
MP2
LVT
b
MN2
LVT
I2
Invertor
VDD
R1004
d
R1005
TBUF1
ENABLE2
E
OUT
IN
DIN
3721
R1000
R1001
AVDD
AVDD
MP1
HVT
c
MN1
HVT
b
R1
I1
GND
AVDD
R1002
a
R1003
ENABLE1
E
OP1
A
P
N
VREF

Fig.12

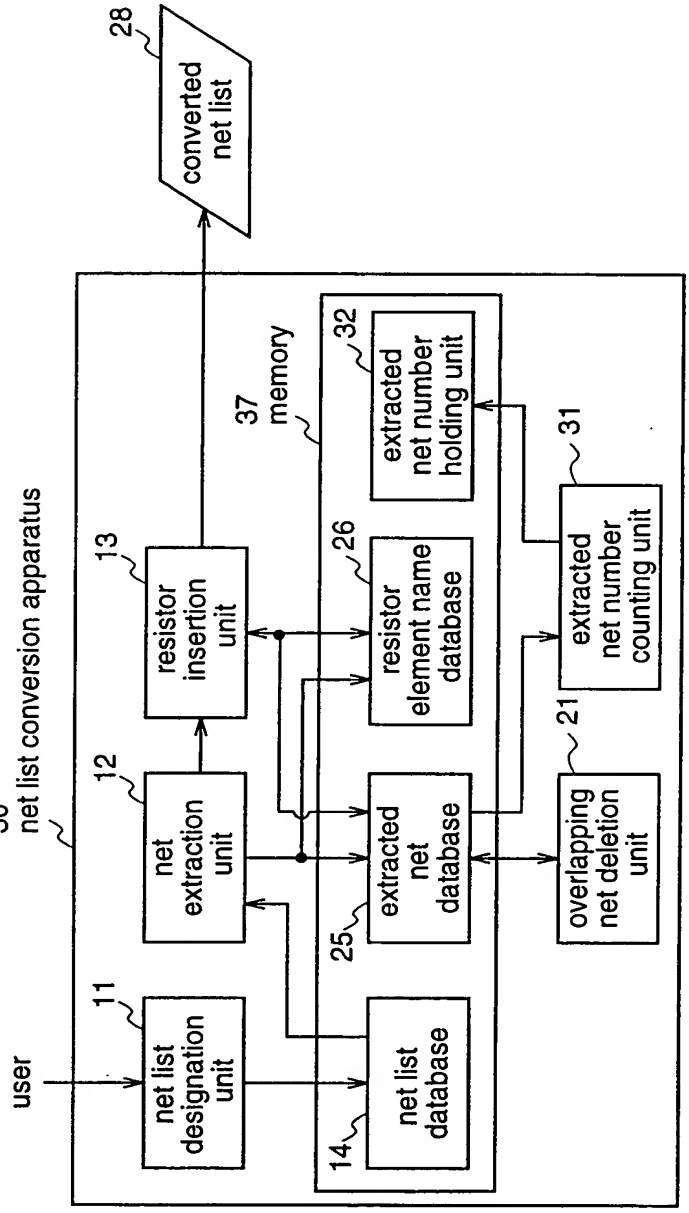
user
30
net list conversion apparatus
11
net list designation unit
12
net extraction unit
13
resistor insertion unit
14
net list database
25
extracted net database
26
resistor element name database
37
memory
32
extracted net number holding unit
21
overlapping net deletion unit
31
extracted net number counting unit
28
converted net list

Fig.13

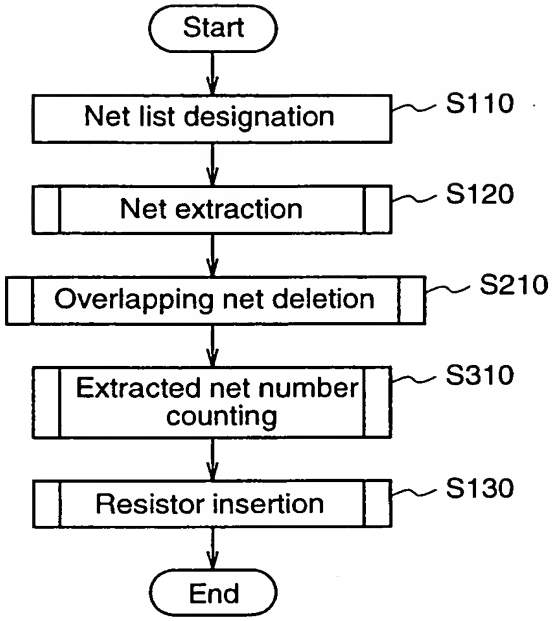

Fig.14

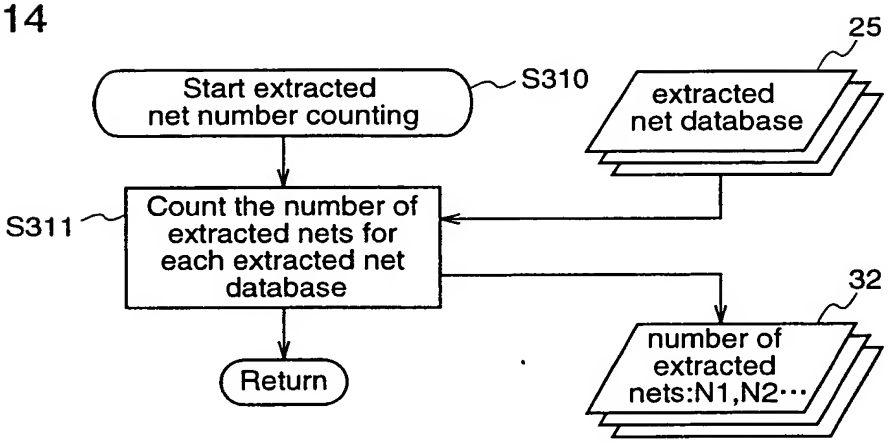

Fig.15

number of extracted nets

AVDD:2
AVDD:2 OP
VDD: 1
VDD: 2 TBUF

32

Fig.16

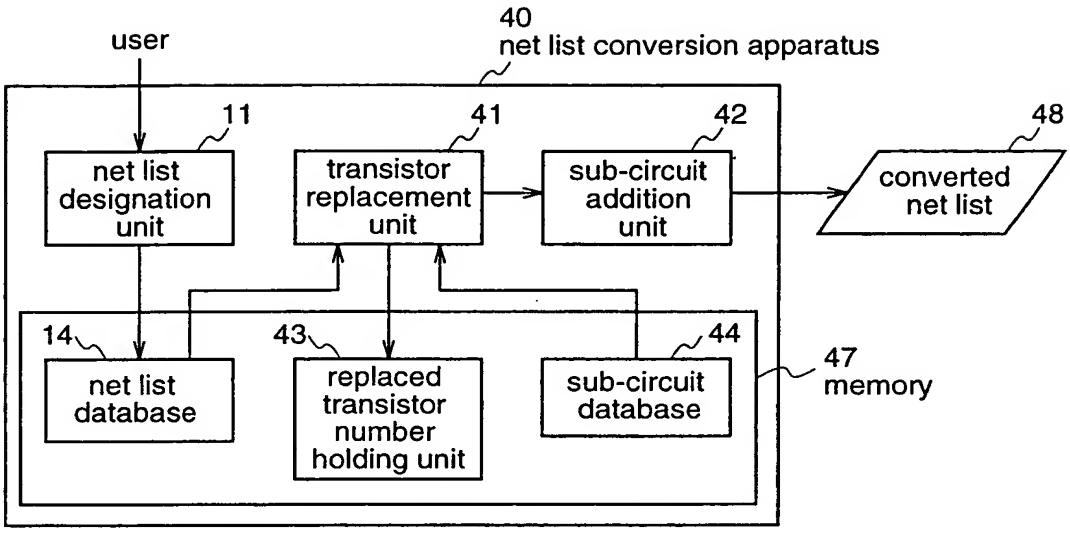
user
40
net list conversion apparatus
11
net list designation unit
41
transistor replacement unit
42
sub-circuit addition unit
48
converted net list
14
net list database
43
replaced transistor number holding unit
44
sub-circuit database
47
memory

Fig.17

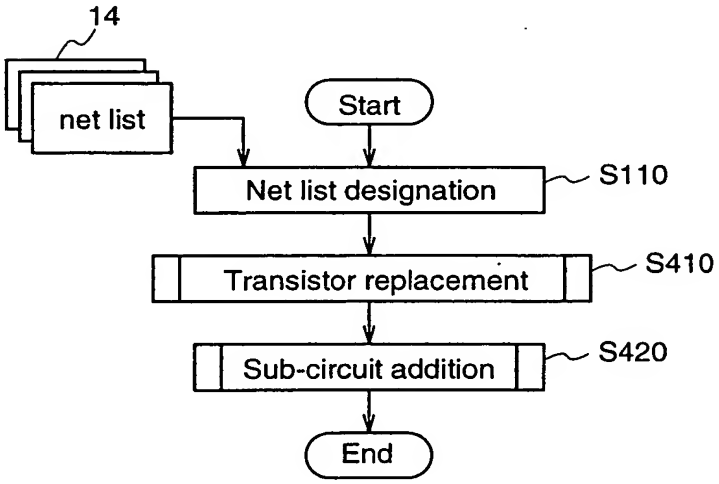
14
net list
Start
Net list designation
S110
Transistor replacement
S410
Sub-circuit addition
S420
End

Fig.18

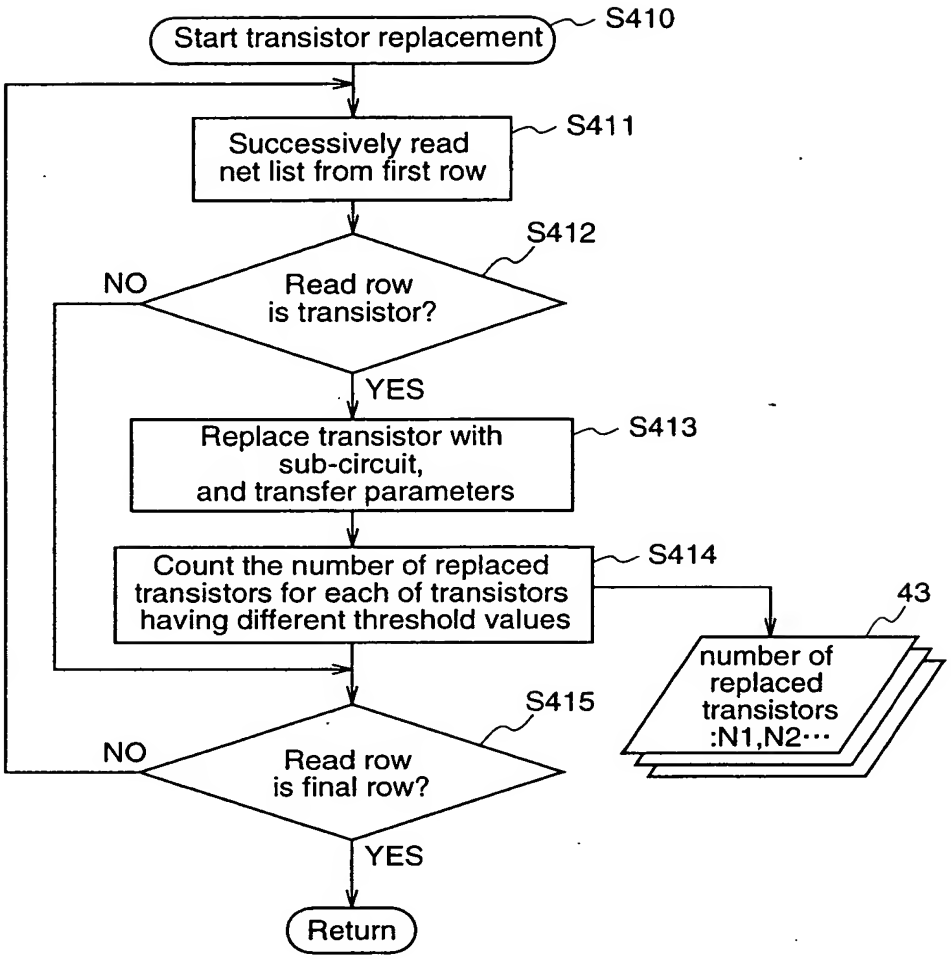
Start transistor replacement
S410
Successively read net list from first row
S411
Read row is transistor?
S412
NO
YES
Replace transistor with sub-circuit, and transfer parameters
S413
Count the number of replaced transistors for each of transistors having different threshold values
S414
43
number of replaced transistors :N1,N2…
Read row is final row?
S415
NO
YES
Return

Fig.19

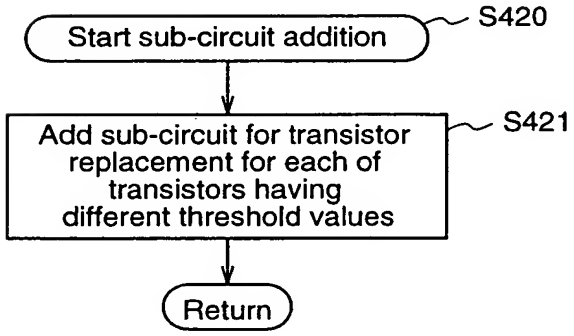
Start sub-circuit addition
S420
Add sub-circuit for transistor replacement for each of transistors having different threshold values
S421
Return

Fig.20

post-conversion net list

```
1.  XMP1 c c AVDD AVDD PHVT PARAMS:LPH=1u, WPH=5u
2.  XMN1 c a b      0      NHVT PARAMS:LNH=1u, WNH=5u
3.  R1   b 0 10k
4.  XOP1 VREF b a ENABLE1 OP
5.
6.  XMP2 DOUT d VDD VDD PLVT PARAMS:LPL=1u, WPL=2u
7.  XMN2 DOUT d 0    0     NLVT PARAMS:LNL=1u, WNL=1u
8.  XTBUF1 DIN d ENABLE2 TBUF
9.
10. .SUBCKT OP P N A E
11. XMP01 1 2 3 4 PHVT PARAMS:LPH=1u, WPH=5u
12. XMN01 5 6 7 8 NHVT PARAMS:LNH=1u, WNH=5u
13.    :
14. .END OP
15.
16. .SUBCKT TBUF IN OUT E
17. XMP01 1 2 3 4 PLVT PARAMS:LPH=1u, WPH=2u
18. XMN01 5 6 7 8 NLVT PARAMS:LNH=1u, WNH=1u
19.    :
20. .END TBUF
21.
22. .SUBCKT PHVT D G S B PARAMS:LPH=1u, WPH=1u
23. MPH D G S B pchhvt l=LPH w=WPH
24. RPH1 G AVDD 100T
25. RPH2 G 0      100T
26. .END PHVT
27.
28. .SUBCKT NHVT D G S B PARAMS:LNH=1u, WNH=1u
29. MNH D G S B nchhvt l=LNH w=WNH
30. RNH1 G AVDD 100T
31. RNH2 G 0      100T
32. .END NHVT
33.
34. .SUBCKT PLVT D G S B PARAMS:LPL=1u, WPL=1u
35. MPL D G S B pchlvt l=LPL w=WPL
36. RPL1 G VDD 100T
37. RPL2 G 0     100T
38. .END PLVT
39.
40. .SUBCKT NLVT D G S B PARAMS:LNL=1u, WNL=1u
41. MNL D G S B nchlvt l=LNL w=WNL
42. RNL1 G VDD 100T
43. RNL2 G 0     100T
44. .END NLVT
45.
46. .end
```

48

number of replaced transistors 43

AVDD:2
AVDD:2 OP:1
VDD: 2
VDD: 2 TBUF:1

Fig.21

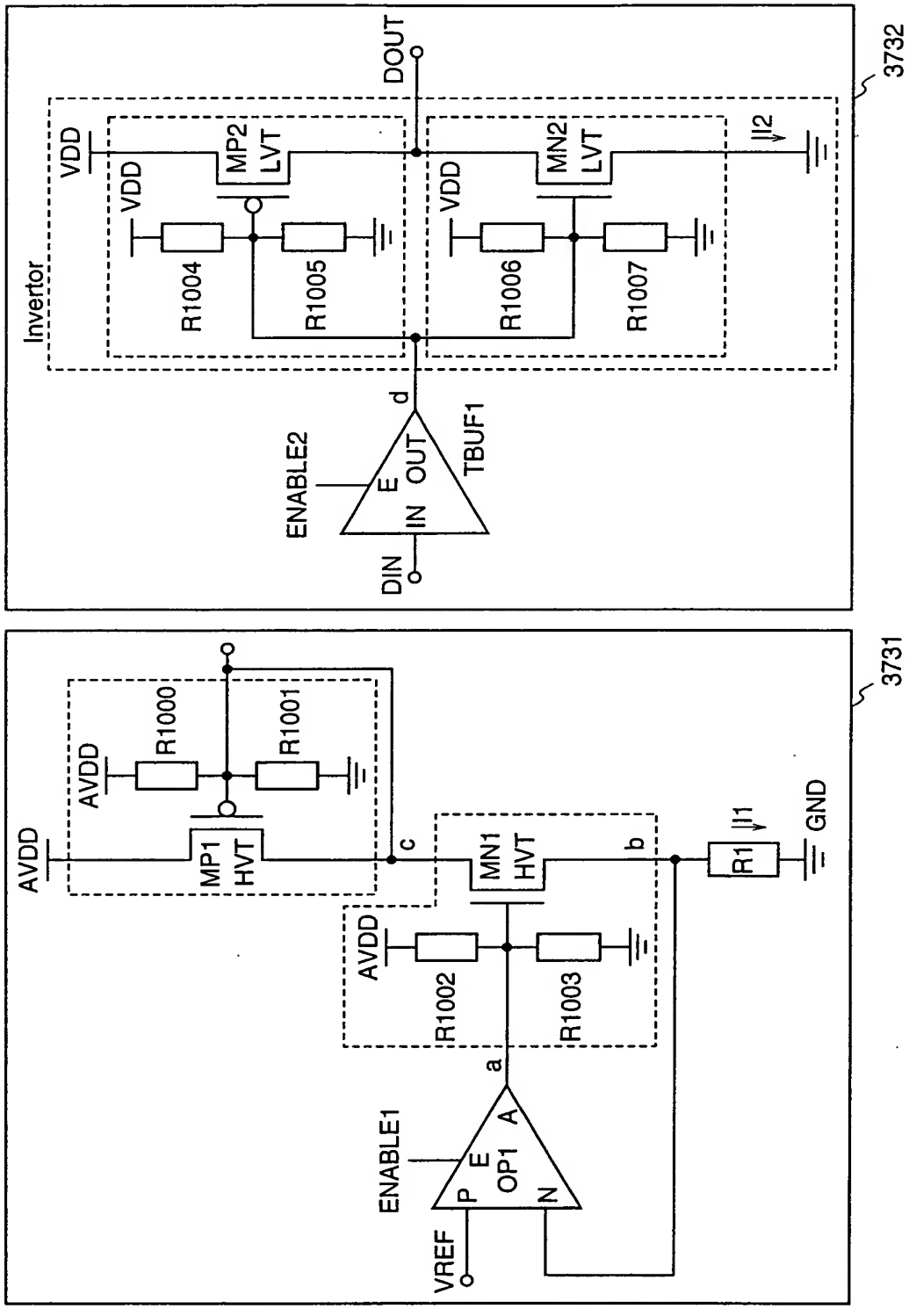
3732
DOUT
VDD
MP2
LVT
MN2
LVT
I2
Invertor
R1004
R1005
R1006
R1007
d
ENABLE2
E
OUT
TBUF1
IN
DIN
3731
AVDD
R1000
R1001
MP1
HVT
c
MN1
HVT
b
R1
I1
GND
R1002
R1003
a
ENABLE1
OP1
A
P
N
VREF

Fig.22

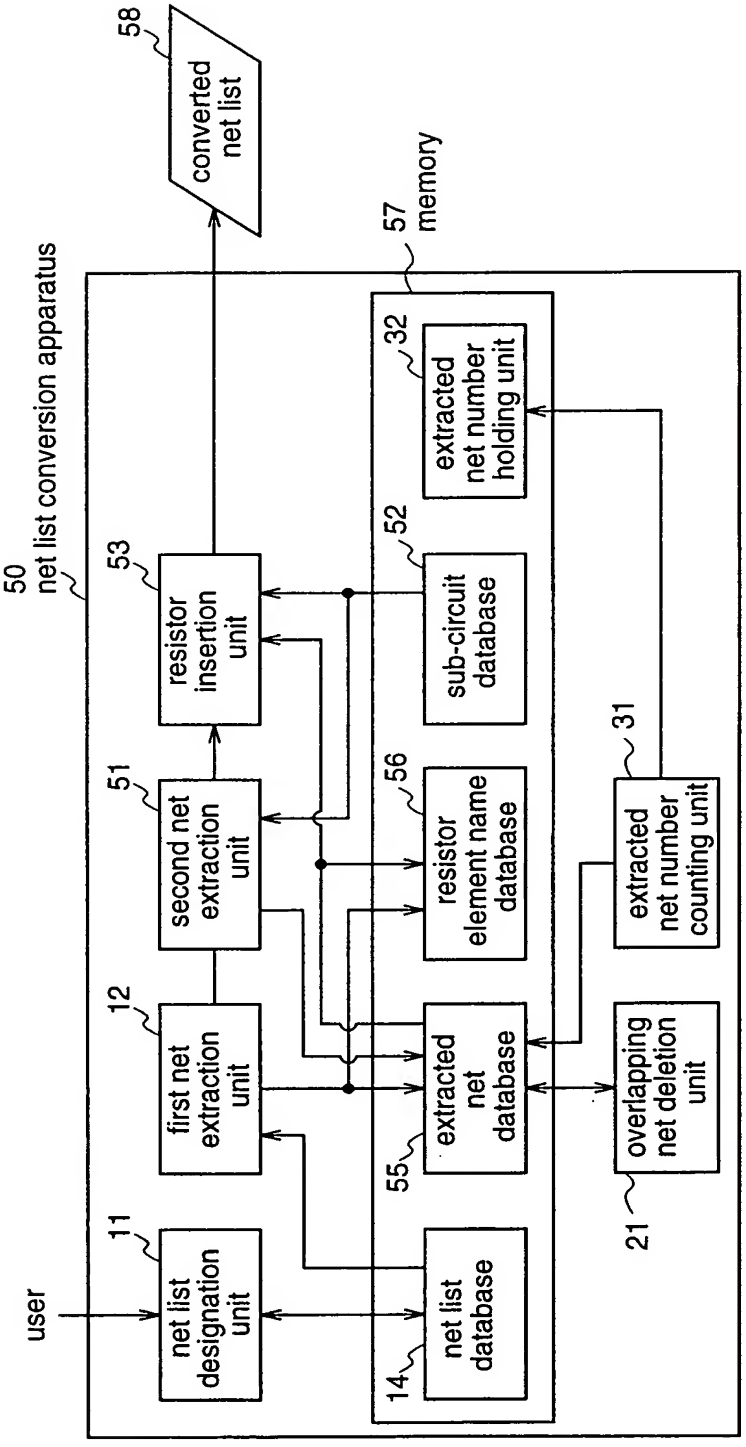
user
50
net list conversion apparatus
11
net list designation unit
12
first net extraction unit
51
second net extraction unit
53
resistor insertion unit
58
converted net list
57
memory
14
net list database
55
extracted net database
56
resistor element name database
52
sub-circuit database
32
extracted net number holding unit
21
overlapping net deletion unit
31
extracted net number counting unit

Fig.23

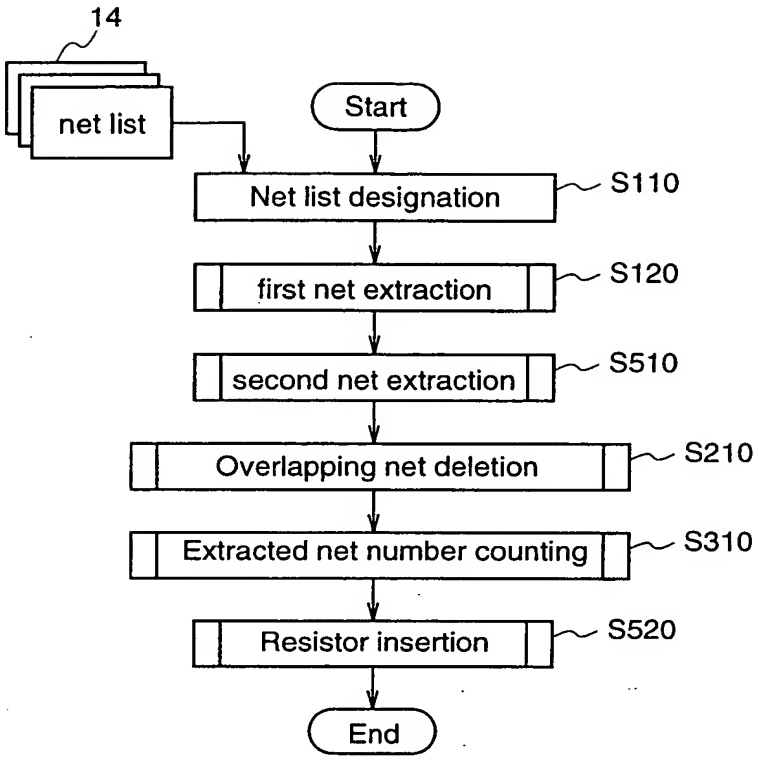
14
net list
Start
Net list designation
S110
first net extraction
S120
second net extraction
S510
Overlapping net deletion
S210
Extracted net number counting
S310
Resistor insertion
S520
End

Fig.24

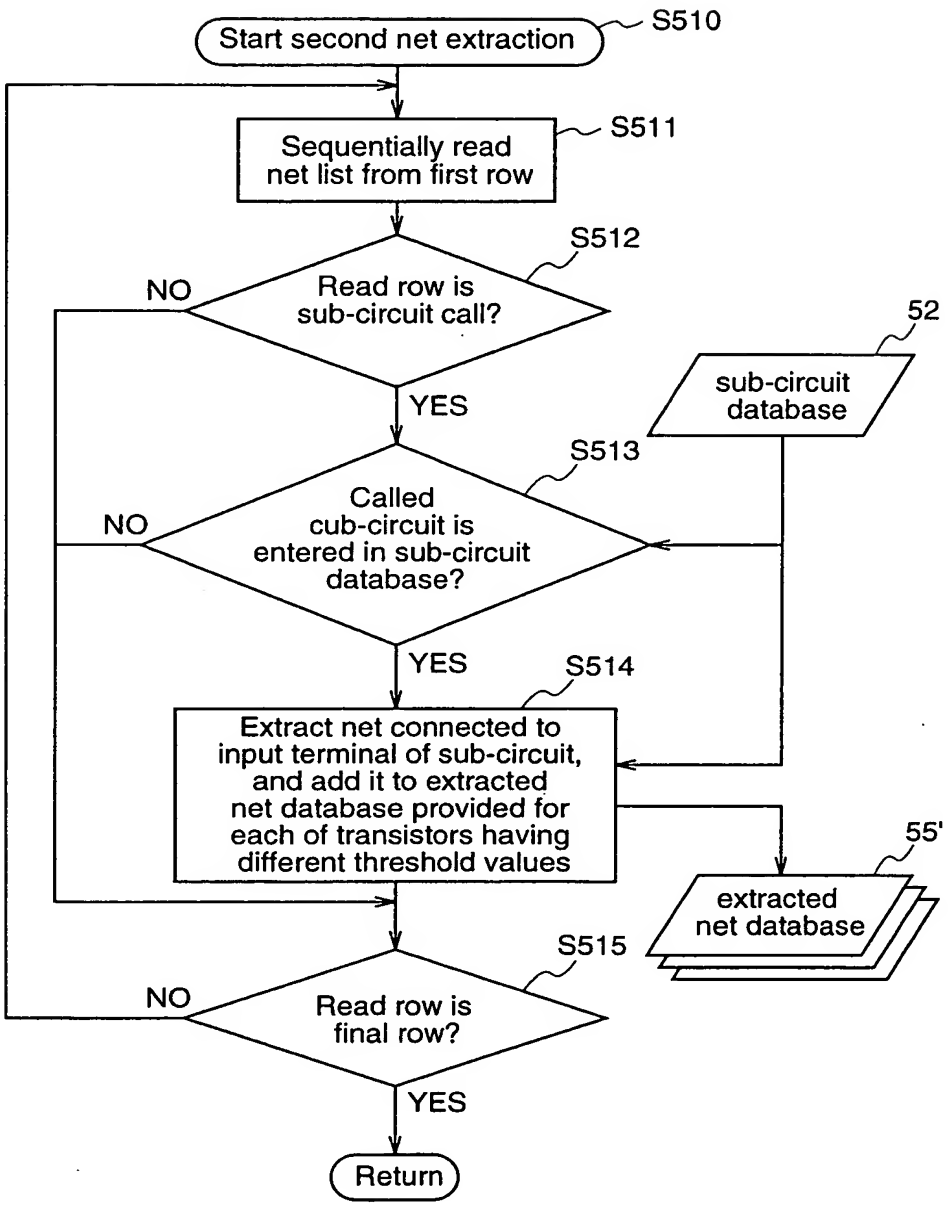
Start second net extraction
S510
Sequentially read net list from first row
S511
Read row is sub-circuit call?
S512
NO
YES
sub-circuit database
52
Called cub-circuit is entered in sub-circuit database?
S513
NO
YES
Extract net connected to input terminal of sub-circuit, and add it to extracted net database provided for each of transistors having different threshold values
S514
extracted net database
55'
Read row is final row?
S515
NO
YES
Return

Fig.25

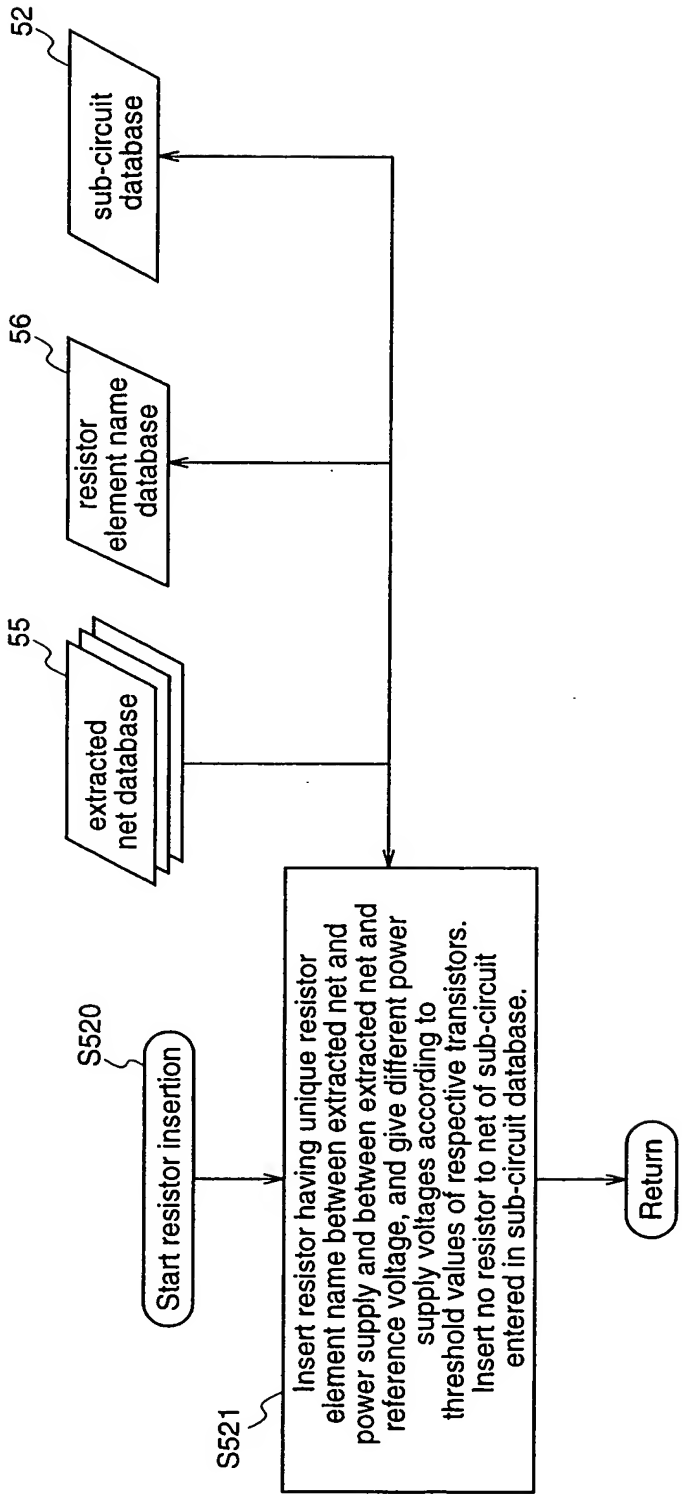
52
sub-circuit database
56
resistor element name database
55
extracted net database
S520
Start resistor insertion
S521
Insert resistor having unique resistor element name between extracted net and power supply and between extracted net and reference voltage, and give different power supply voltages according to threshold values of respective transistors. Insert no resistor to net of sub-circuit entered in sub-circuit database.
Return

Fig.26(a)

target net list

```
1.    MP1 c c AVDD AVDD pchhvt l=1u w=5u
2.    MN1 c a b      0     nchhvt l=1u w=5u
3.    R1   b 0 10k
4.    XOP1 VREF b a ENABLE1 OP
5.
6.    XINV1 d DOUT INV
7.    XTBUF1 DIN d ENABLE2 TBUF
8.
9.    .SUBCKT OP P N A E
10.   MP01 1 2 3 4 pchhvt l=1u w=5u
11.   MN01 5 6 7 8 nchhvt l=1u w=5u
12.      :
13.   .END OP
14.
15.   .SUBCKT TBUF IN OUT E
16.   MP01 1 2 3 4 pchlvt l=1u w=2u
17.   MN01 5 6 7 8 nchlvt l=1u w=1u
18.      :
19.   .END TBUF
20.
21.   .SUBCKT INV IN OUT
22.   MP2 OUT IN VDD VDD pchlvt l=1u w=2u
23.   MN2 OUT IN 0     0    nchlvt l=1u w=1u
24.   .END INV
25.
26.   .end
```

Fig.26(b)

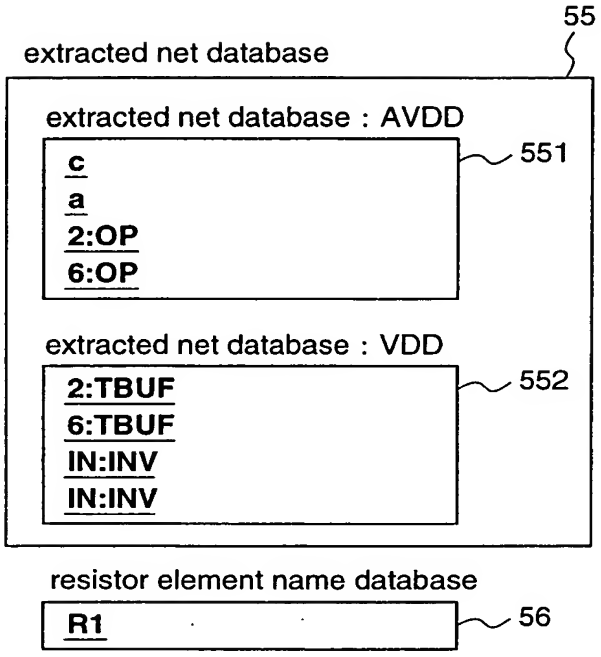

Fig.26(c)

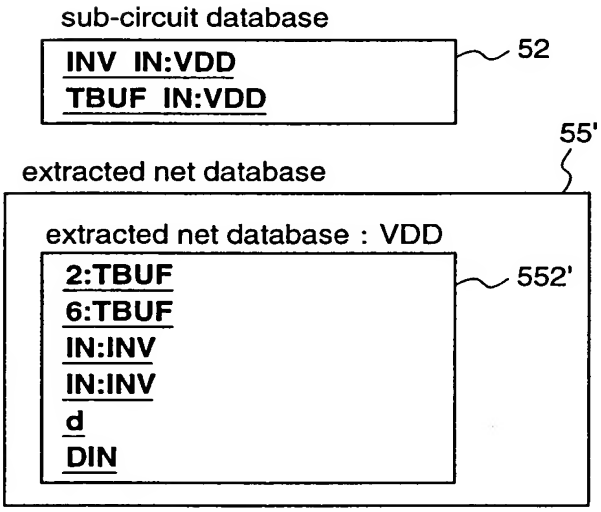

Fig.26(d)

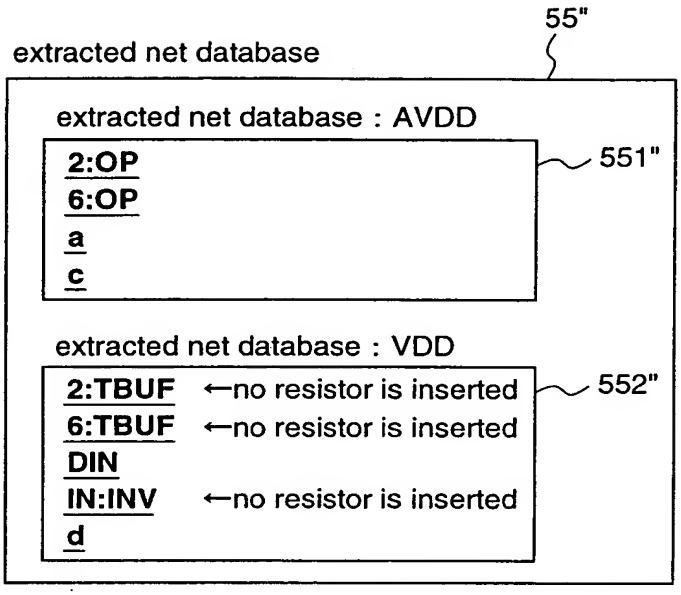

Fig.26(e)

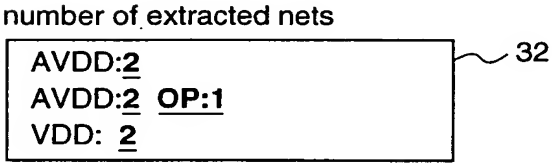

Fig.26(f)

post-conversion net list

58

```
1.   MP1 c c AVDD AVDD pchhvt l=1u w=5u
2.   MN1 c a b      0      nchhvt l=1u w=5u
3.   R1   b 0 10k
4.   XOP1 VREF b a ENABLE1 OP
5.
6.   XINV1 d DOUT INV
7.   XTBUF1 DIN d ENABLE2 TBUF
8.
9.   .SUBCKT OP P N A E
10.  MP01 1 2 3 4 pchhvt l=1u w=5u
11.  MN01 5 6 7 8 nchhvt l=1u w=5u
12.     :
13.  R0P000 2 AVDD 100T
14.  R0P001 2 0      100T
15.  R0P002 6 AVDD 100T
16.  R0P003 6 0      100T
17.  .END OP
18.
19.  .SUBCKT TBUF IN OUT E
20.  MP01 1 2 3 4 pchlvt l=1u w=2u
21.  MN01 5 6 7 8 nchlvt l=1u w=1u
22.     :
23.  .END TBUF
24.
25.  .SUBCKT INV IN OUT
26.  MP2 DOUT d VDD VDD pchlvt l=1u w=2u
27.  MN2 DOUT d 0    0      nchlvt l=1u w=1u
28.  .END INV
29.
30.  R1000 c AVDD 100T
31.  R1001 c 0      100T
32.  R1002 a AVDD 100T
33.  R1003 a 0      100T
34.  R1004 d VDD   100T
35.  R1005 d 0      100T
36.  R1006 DIN VDD  100T
37.  R1007 DIN 0      100T
38.
39.  .end
```

56'

resistor element name database

```
R1
R0P000:OP
R0P001:OP
R0P002:OP
R0P003:OP
R1000
R1001
R1002
R1003
R1004
R1005
R1006
R1007
```

Fig.27

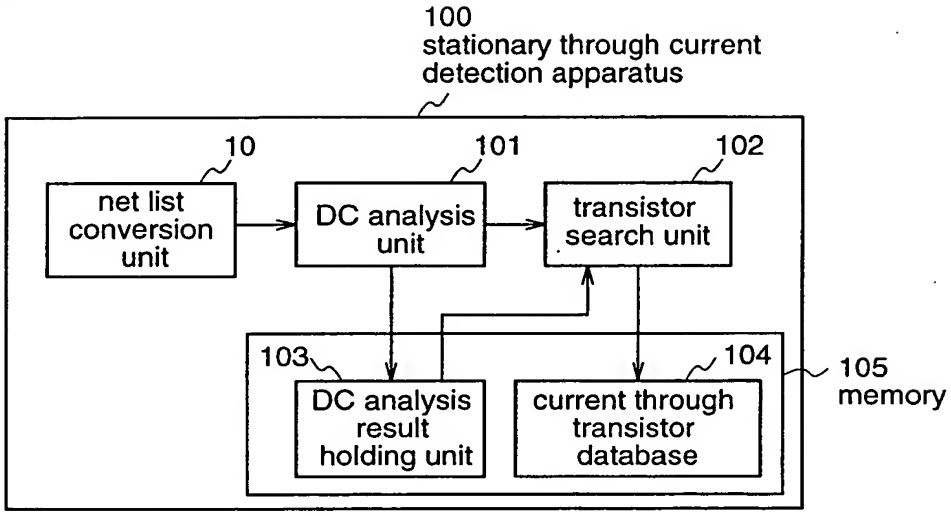
100
stationary through current detection apparatus
10
net list conversion unit
101
DC analysis unit
102
transistor search unit
103
DC analysis result holding unit
104
current through transistor database
105
memory

Fig.28

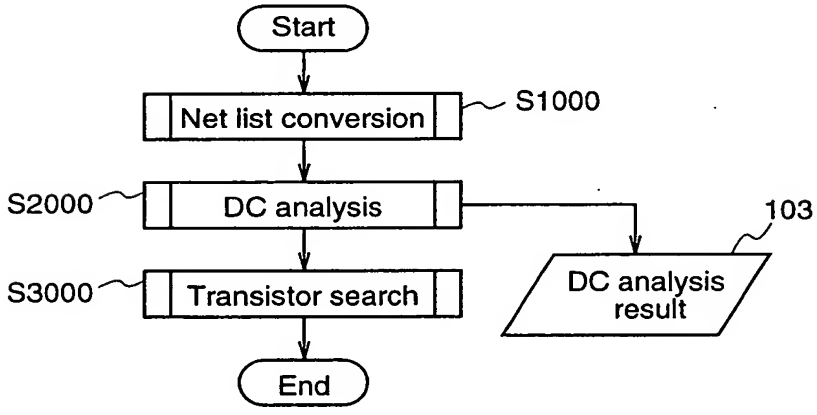
Start
Net list conversion
S1000
S2000
DC analysis
103
DC analysis result
S3000
Transistor search
End

Fig.29

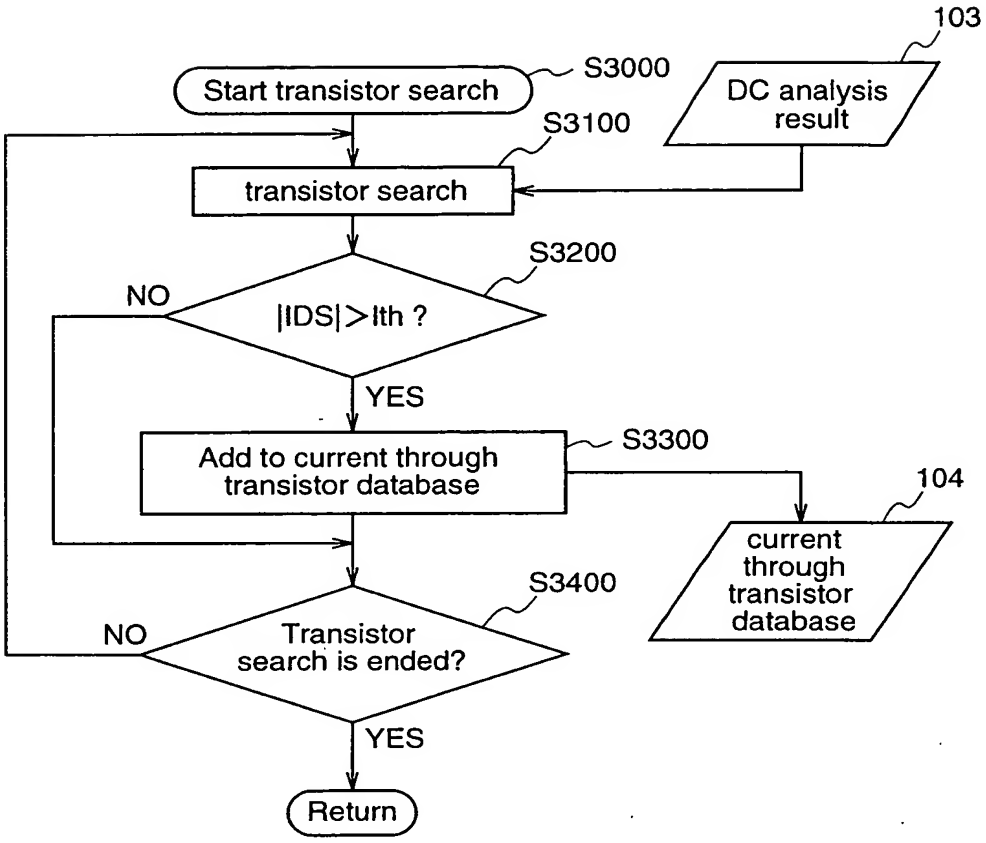
103
DC analysis result
Start transistor search
S3000
S3100
transistor search
S3200
NO
|IDS|>Ith ?
YES
Add to current through transistor database
S3300
104
current through transistor database
S3400
NO
Transistor search is ended?
YES
Return

Fig.30

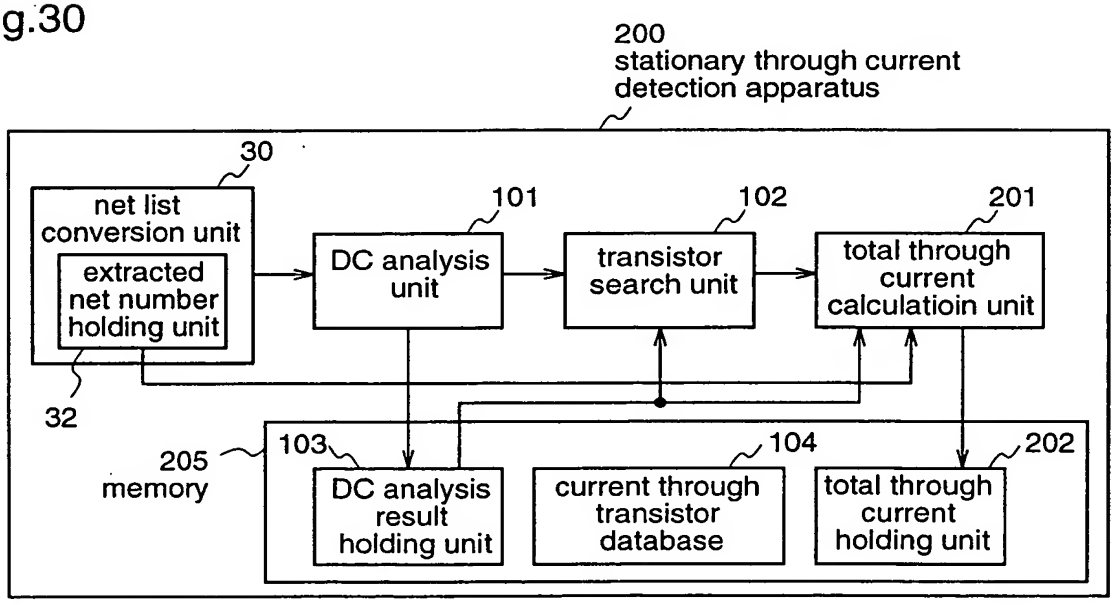
200
stationary through current detection apparatus
30
net list conversion unit
extracted net number holding unit
32
101
DC analysis unit
102
transistor search unit
201
total through current calculatioin unit
205
memory
103
DC analysis result holding unit
104
current through transistor database
202
total through current holding unit

Fig.31

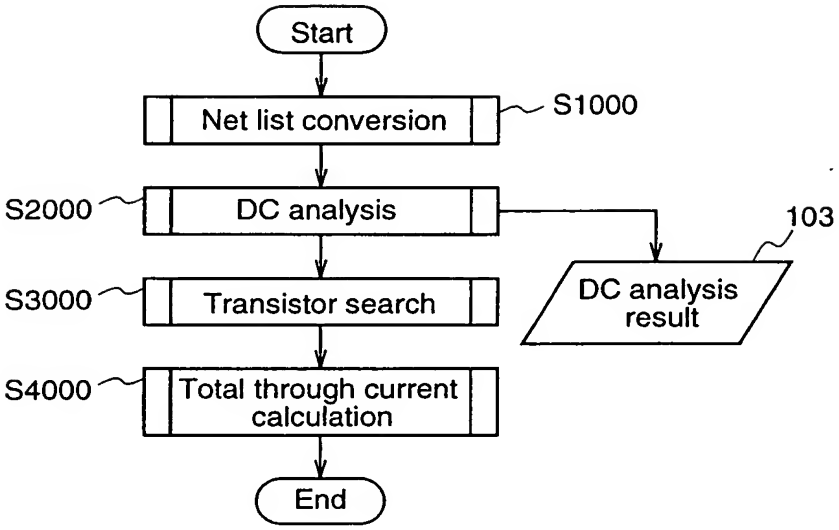
Start
Net list conversion
S1000
S2000
DC analysis
103
DC analysis result
S3000
Transistor search
S4000
Total through current calculation
End

Fig.32

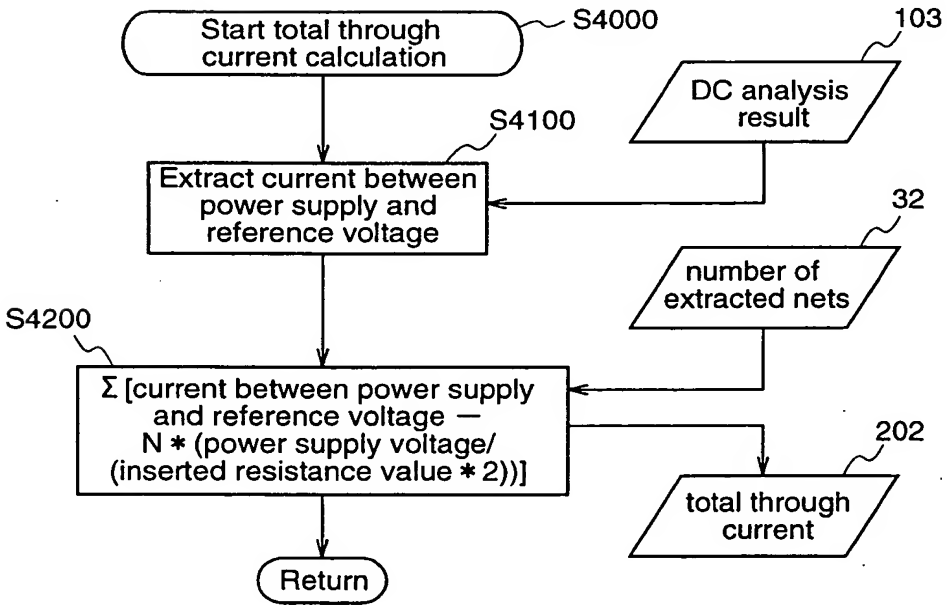
Start total through current calculation
S4000
103
DC analysis result
S4100
Extract current between power supply and reference voltage
32
number of extracted nets
S4200
Σ [current between power supply and reference voltage — N * (power supply voltage/ (inserted resistance value * 2))]
202
total through current
Return

Fig.33

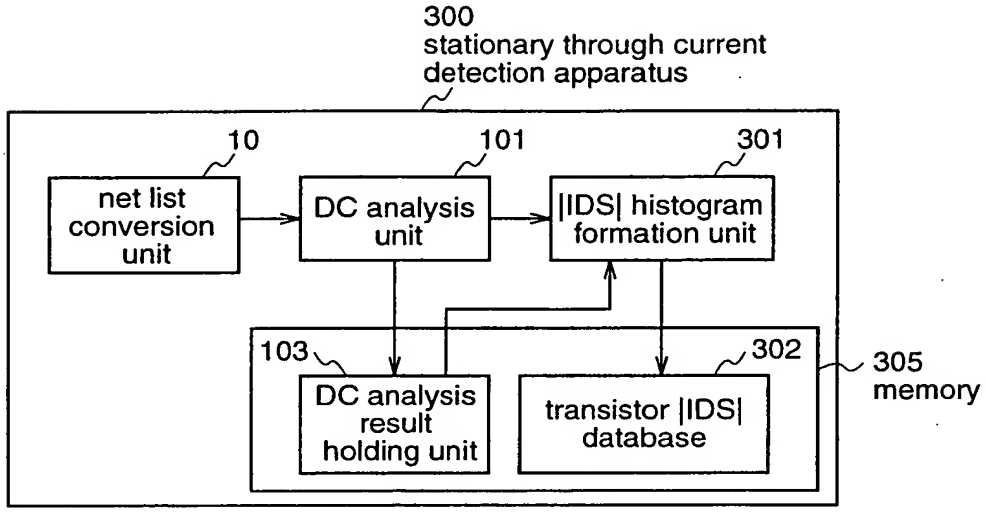
300
stationary through current detection apparatus
10
net list conversion unit
101
DC analysis unit
301
|IDS| histogram formation unit
103
DC analysis result holding unit
302
transistor |IDS| database
305
memory

Fig.34

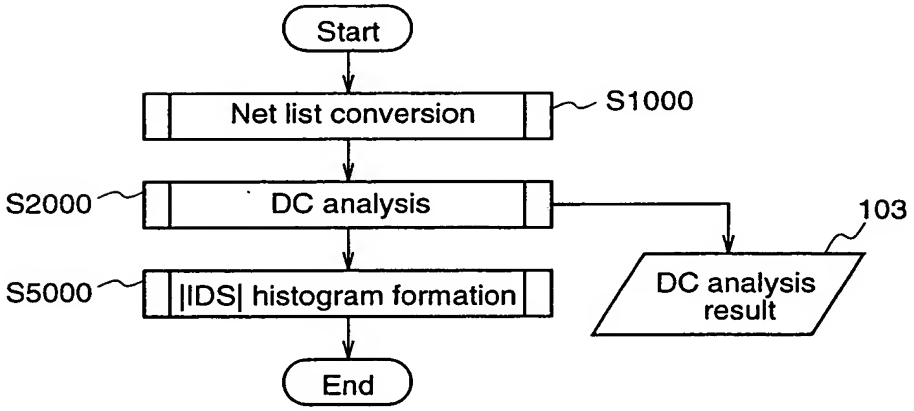
Start
Net list conversion
S1000
S2000
DC analysis
S5000
|IDS| histogram formation
End
103
DC analysis result

Fig.35

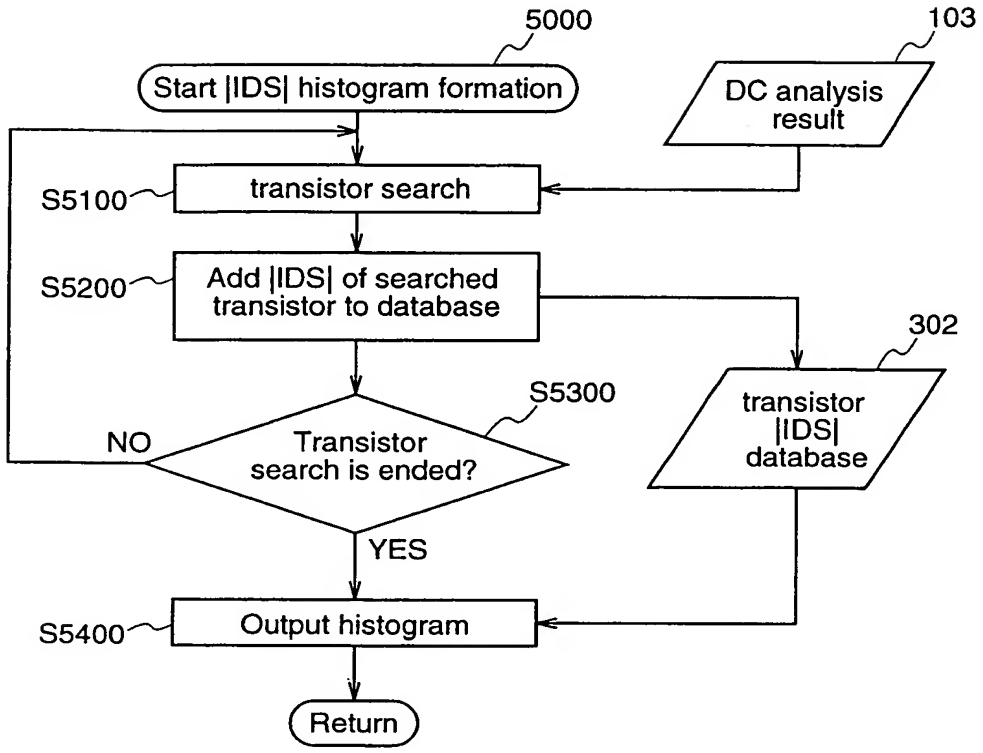

Fig.36(a)

transistor |IDS| database

302

20 μA	MP1
20 μA	MN1
5 μA	MP2
5 μA	MN2
1nA	OP1/MP01
1nA	OP1/MN01
1nA	INV1/MP2
1nA	INV1/MP2
1nA	TBUF1/MP01
1nA	TBUF1/MP01

Fig.36(b)

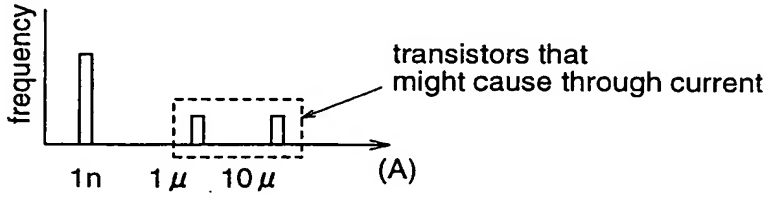

Fig.37(a)

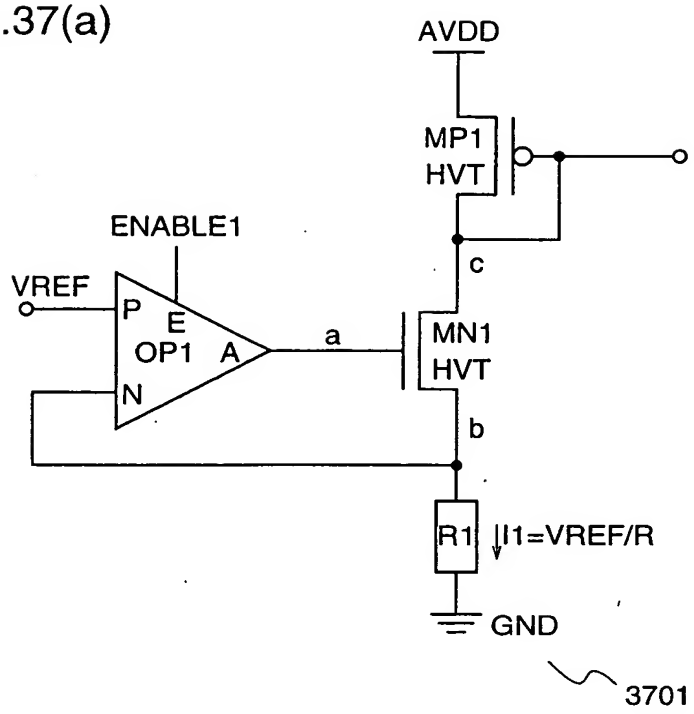

Fig.37(b)

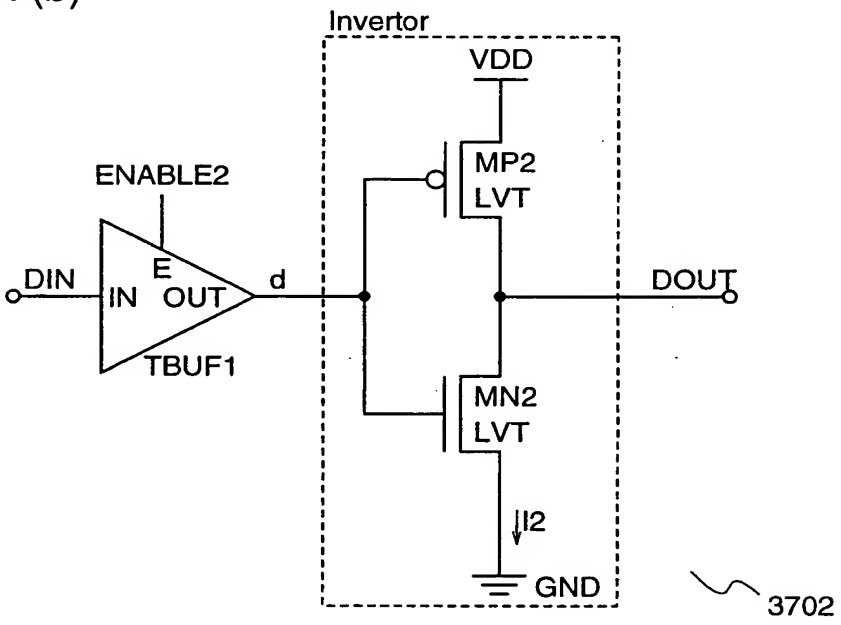

Fig.38